Amendments to the Claims:

Please amend Claims 1, 7, 12, and 18 as follows:

1. (currently amended) A serial, multiplexed communications system comprising:

a bus controller comprising a processor for issuing a plurality of commands or messages, wherein the commands or messages are issued in a serial manner;

a plurality of data channels for performing predefined functions in response to the commands or messages;

a common digital bus interconnecting said bus controller and said plurality of data channels for supporting serial communication therebetween; and

a plurality of network device interfaces, one of which is associated with each data channel for interconnecting said respective data channel with said common digital bus and communicating information from said bus controller to said data channel, wherein at least one of said network device interfaces comprises a state machine and does not comprise a general processor ~~such that said network device interface communicates with said bus controller independent of use of a processor~~, and wherein said plurality of network device interfaces are connected to the common digital bus in parallel to perform predefined functions as parallel processes to thereby support high speed communication over said common digital bus.

2. (previously presented) A serial, multiplexed communications system according to Claim 1 wherein said bus controller generates a synchronous clock signal which is provided to said network device interface such that said network device interface operates using the synchronous clock signal provided by said bus controller.

3. (original) A serial, multiplexed communications system according to Claim 1 wherein the plurality of data channels are selected from the group consisting of sensors and actuators.

4. (original) A serial, multiplexed communications system according to Claim 1 wherein said network device interface comprises a receiver for receiving messages from said bus controller via said common digital bus.

5. (original) A serial, multiplexed communications system according to Claim 1 wherein said network device interface comprises a device interface for providing commands to a data channel connected thereto and for receiving data from the associated data channel.

6. (original) A serial, multiplexed communications system according to Claim 1 wherein said network device interface comprises a transmitter for transmitting messages to said bus controller via said common digital bus.

7. (currently amended) A serial, multiplexed communications system according to Claim 1, wherein said network device interface communicates with both said processor of said bus controller and a data channel connected to said network device interface~~, wherein said network device interface operates independent of a processor when communicating with said processor of said bus controller~~.

8. (original) A serial, multiplexed communications system according to Claim 1 wherein said network device interface is an Application Specific Integrated Circuit (ASIC).

9. (original) A serial, multiplexed communications system according to Claim 1 wherein said network device interface receives commands from said bus controller and controls the data channel connected to said network device interface based on the command.

10. (original) A serial, multiplexed communications system according to Claim 1 wherein said network device interface receives data from said bus controller and provides the data to the data channel connected to said network device interface.

11. (original) A serial, multiplexed communications system according to Claim 1 wherein said network device interface receives data from the data channel connected to said

network device interface, and wherein said network device interface sends the data to said bus controller.

12. (currently amended) A network device interface adapted to interconnect an associated data channel with a processor of a bus controller via a common serial, multiplexed, digital bus, the interface comprising:

a receiver for receiving messages from the bus controller via the common digital bus, wherein the messages are issued from the bus controller in a serial manner;

a device interface for providing commands to the associated data channel in response to messages received by said receiver and for receiving data from the associated data channel; and

a transmitter for transmitting messages to the bus controller via the common digital bus,

wherein said network device interface is a state machine and does not comprise a general processor, ~~such that said network device interface communicates with said bus controller independent of use of a processor~~

wherein said network device interface is one of a plurality of network device interfaces connected to the common digital bus in parallel to perform predefined functions as parallel processes to thereby support high speed communication over said common digital bus.

13. (previously presented) A network device interface according to Claim 12 wherein said network device interface operates using a synchronous clock signal provided by said bus controller.

14. (original) A network device interface according to Claim 12 wherein said receiver receives synchronous clock signals from the bus controller via a common clock bus, and wherein said transmitter transmits messages in synchronization with the synchronous clock signals to the bus controller via the common digital bus.

15. (original) A network device interface according to Claim 12 wherein said receiver receives messages at a bit rate for a predetermined set of bit rates, and wherein said transmitter transmits messages at the same predetermined bit rate to the bus controller via the common digital bus.

16. (original) A network device interface according to Claim 12 wherein said receiver receives messages comprised of a plurality of bits having a value defined by a transition between first and second states, and wherein said device interface provides commands to the associated data channel at a predetermined time relative to the transition that defines the value of a respective bit of the message.

17. (original) A network device interface according to Claim 12 wherein said receiver receives messages comprised of a plurality of bits, wherein said receiver further receives a synchronous clock signal comprised of a plurality of clock pulses, and wherein said device interface provides commands to the associated data channel at a predetermined time as defined by a respective clock pulse which, in turn, is defined based upon a predetermined relationship to a respective bit of the message.

18. (currently amended) A serial, multiplexed communications system comprising:

a bus controller comprising a processor for issuing a plurality of commands, wherein the messages are issued from the bus controller in a serial manner;

at least one data channel for performing predefined functions in response to the commands;

a common digital bus interconnecting said bus controller and said data channel for supporting communication therebetween; and

a network device interface connected to said data channel for interconnecting said respective data channel with said common digital bus and communicating information from said bus controller to said data channel, wherein said network device interface comprises a state machine and does not comprise a general processor, ~~such that said network device interface communicates with said bus controller independent of use of a processor,~~

wherein said network device interface is one of a plurality of network device interfaces connected to the common digital bus in parallel to perform predefined functions as parallel processes to thereby support high speed communication over said common digital bus.

19. (original) A serial, multiplexed communications system according to Claim 18, wherein said network device interface provides commands from said bus controller to a data channel connected thereto and receives data from the associated data channel and transmits the data to said bus controller.

20. (previously presented) A serial, multiplexed communications system according to Claim 18 wherein said bus controller generates a synchronous clock signal which is provided to said network device interface such that said network device interface operates using the synchronous clock signal provided by said bus controller.